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Objections

The Examiner has rejected the title of the invention requiring us to choose a new title indicative of the invention to which the claims are directed. The title has accordingly been amended, and approval by the Examiner is respectively requested. Additionally, the Examiner objects to claim 40 for an informality, which has been taken care of by amendment.

35 U.S.C. §112

Claims 20-22 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for the reasons noted in the official action. The rejected claims are accordingly amended, by the above claim amendments, and the presently pending claims are now believed to particularly point out and distinctly claim the subject matter regarded as the invention, thereby overcoming all of the raised §112, second paragraph, rejections.

35 U.S.C. § 102(b)

Claims 12, 19-22, 24, 25, 33, 34, 36-38, 73, 74 and 76 are rejected under 35 U.S.C. §102(b) as being anticipated by Hong (US 5,770,501). Accordingly, the claims have been amended to recite features neither disclosed nor suggested by the cited prior art. In particular, independent claims 12, 19, 21, 24, 25, 33, and 73 now recite the feature of at least one sloped trench, having a base and an opening wider than the base. Support for this amendment is provided for by FIG. 2, therefore no new matter has been entered.

35 U.S.C. § 103(a)

Claim 40 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hong in view of Yoo et al (US 5,747,848). Accordingly, claim 40 has been amended to recite features neither disclosed nor suggested by the cited prior art. In particular, claim 40 now recites the feature of at least one sloped trench. Support for this amendment is provided for by the specification and drawings, therefore no new matter has been entered.

As pointed out by the Examiner, Hong fails to disclose a nonvolatile memory having a conductive bit line connected to the drain of each memory cell in a row in conjunction with a

common source line, otherwise known as the NOR configuration. Accordingly, to further define the present invention over Hong, the amended independent claims are now directed to nonvolatile memory having a NOR structure comprising, among other things, at least one sloped trench which is disclosed by FIGS. 1A and 2. Hong neither discloses nor suggests such features. Yoo et al. is cited for teaching a conductive bit line which is connected to the drain of each memory cell in a row in conjunction with a common source line. Accordingly, neither Yoo et al. nor any other cited references cure the deficiency of Hong regarding sloped trenches.

Additionally, the present invention is directed to reducing the size of the memory cell while addressing the capacitive coupling issues. In particular, inadequate capacitive coupling between the control gate and the floating gate inhibits proper operation of the memory cell. However, manufacturing issues must also be addressed when reducing the size of the memory cell. It is to be appreciated that leading edge isolation trenches on the order of about 0.15 to about 0.18 mm wide are currently in production. Development evaluations targeting 0.13 mm and lower design rules are taking place with structure widths to less than 0.10 mm. This reduction in trench width challenges all aspects of the isolation integration including etch, liner deposition, and the ability of the fill oxide to provide a void free fill and uniform oxide characteristics across 200 and 300 mm substrates. Having a sloped trench with a base and an opening wider than the base as recited by the amended claims provides a larger trench opening which facilities a simpler oxide fill process than the liquid phase deposition technique taught by Hong, which is used to fill his vertically sided trenches.

Furthermore, other performance issues must also be addressed when reducing the size of the memory cell. In particular, as the isolation spacing between active devices continues to shrink below 180nm, punch-through and latch-up becomes problematic. However, having a sloped trench as recited by the amended claims increases the distance of travel for electrical field lines thereby providing better isolation to prevent punch-through and providing better latch-up immunity than the vertically sided trenches of Hong. None of the above noted advantageous are taught by Hong or any of the other cited references for having slope trenches. Accordingly, amended claim 40 would not have been obvious to one of ordinary skill in the art at the time the invention was made in view of the teachings of the cited prior art references.

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CONCLUSION

Applicants respectfully submit that, in view of the above remarks, the application is now in condition for allowance. Applicants respectfully request that claims 12, 19-22, 24, 25, 33, 34, 36-38, 40, 73, 74, and 76 be passed to allowance. If the Examiner has any questions or comments regarding the present application, please contact the undersigned at the telephone number indicated below.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, L.L.P.

By _____
William A. Jividen
Registration No. 42,695

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724
jividenw@kghs.com

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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE OF THE INVENTION

Please amend the title as follows:

STACKED GATE REGION OF A NONVOLATILE MEMORY CELL HAVING A NOR STRUCTURE ~~SELF-ALIGNED FLOATING GATE FLASH CELL SYSTEM AND METHOD~~

IN THE CLAIMS

Please amend the claims as follows:

12. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

at least one ~~trench~~sloped trench formed in said substrate, said at least one sloped trench having a base and an opening wider than said base;

field oxide deposited in said at least one ~~trench~~sloped trench and extending above an upper surface of said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one polysilicon ear formed on said at least one floating gate layer and adjacent to said field oxide.

19. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

a plurality of ~~trench~~sloped trenches formed in said substrate, said sloped trenches each having a base and an opening wider than said base;

respective field oxide regions formed in said ~~trench~~sloped trenches;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon ears formed adjacent to corresponding ones of said field oxide regions on said floating gate layer and projecting substantially perpendicular to an upper surface of the floating gate layer.

20. (Amended) The stacked gate region of claim 19, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon earswings for each of the plurality of floating gates.

21. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

a plurality of trenchsloped trenches formed in said substrate, said sloped trenches each having a base and an opening wider than said base;

respective field oxide regions formed in said trenchsloped trenches;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon ears adjacent to a portion of said floating gate layer.

22. (Amended) The stacked gate region of claim 21, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon earswings for each of the plurality of floating gates.

24. (Amended) A nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

at least one trenchsloped trench formed in said substrate, said at least one sloped trench having a base and an opening wider than said base;

a drain formed in said substrate;

a source formed in said substrate;

field oxide deposited in said at least one trenchsloped trench and extending above an upper surface of said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said tunnel oxide layer;

at least one polysilicon ear formed on said at least one floating gate layer and adjacent to said field oxide;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

25. (Amended) A nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

at least one ~~trench~~sloped trench formed in said substrate, said at least one sloped trench having a base and an opening wider than said base;

a drain formed in said substrate;

a source formed in said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said oxide layer;

field oxide deposited in said at least one ~~trench~~sloped trench;

at least one polysilicon ear formed on said at least one floating gate layer;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

33. A nonvolatile memory device having a NOR structure comprising:

a source formed in a substrate;

a drain formed in the substrate;

a floating gate formed over the substrate;

a field oxide deposited in at least one sloped trench formed in the substrate, said at least one sloped trench having a base and an opening wider than said base; and

an ear formed over the substrate.

34. The memory device of claim 33, wherein the ear is comprised of polysilicon.

36. The memory device of claim 33, wherein the ear extends substantially beyond bounds of the floating gate.

37. (Amended) The memory device of claim 33, wherein near vertical sides of the ear do not contact the floating gate.

38. (Amended) The memory device of claim 33, wherein a near vertical edge the ear is adjacent the field oxide and a bottom edge of the ear is adjacent the floating gate.

40. (Amended) A nonvolatile memory device having a NOR structure comprising:

a plurality of memory cells having a plurality of rows, each memory cell comprising:

_____a control gate, associated with a row, formed integral to a common word line associated with the row~~,~~;

_____a source formed in a common region with a source of an adjacent memory cell~~,~~;

_____a drain formed in another common region with a drain of an adjacent memory cell~~,~~;

_____a floating gate deposited in at least one sloped trench formed in the common region between the source and the drain, said at least one sloped trench having a base and an opening wider than said base~~,~~; and

_____a pair of ears;~~and~~

a common source line formed from the common region of the plurality of memory cells; and

a conductive bit line ~~connecting~~ connected to the drain of each memory cell of the row.

73. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a field oxide region deposited in at least one sloped trench formed in a substrate, said at least one sloped trench having a base and an opening wider than said base;

a tunnel oxide layer formed on the substrate adjacent the field oxide region;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one polysilicon structure formed adjacent to said at least one floating gate layer, said polysilicon structure is adapted to increase capacitive coupling of said memory cell.

74. The stacked gate region of claim 73 wherein said polysilicon structure is selected from the group consisting of at least one wing and at least one ear.

76. The stacked gate region of claim 74 wherein said polysilicon structure is at least one ear, said ear being formed adjacent to said field oxide region.